



☐ Drafts
☐ Pending
☒ Active

☒ I1: (520) (205/123).CCLs.
☒ I2: (210310) high adj density
☒ I3: (96949) low adj density
☒ I4: (31468) 12 same 13
☒ I5: (6) 14 and 11

☒ Failed
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☒ Trash

14 and 11

☒ Print
☒ Highlight all the terms fully

Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor	U	S	C	P	I	PT
1	US 20030221967/20031204	8	Via filling method	205/103	205/105; 205/123;	Tsuchida, Hideki et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
2	US 6835294 B2	20041228	Electrolytic copper plating method	205/98	205/101; 205/102;	Tsuchida; Hideki et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
3	US 6761814 B2	20040713	Via filling method	205/118	205/103; 205/123;	Kusaka; Masaru et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
4	US 6440289 B1	20020827	Method for improving seed layer electroplating for semiconductor	205/103	205/102; 205/104;	Woo; Christy Mei-Chu et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
5	US 6107186 A	20000822	High planarity high-density in-laid metallization patterns by damascene-CMP	438/633	205/103; 205/104;	Brd; Darrell M.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
6	US 5503731 A	19960402	Method for producing electrodes of semiconductor device	205/98	205/123; 205/124;	Konuma; Toshimitsu et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>